

## CLAIMS

1. A method of updating a cache in an integrated circuit comprising:  
the cache  
5 a processor connected to the cache via a cache bus;  
a memory interface connected to the cache via a first bus and to the processor via a second bus, the  
first bus being wider than the second bus or the cache bus; and  
memory connected to the memory interface via a memory bus;  
the method comprising the steps of:  
10 (a) following a cache miss, using the processor to issue a request for first data via a first address, the first  
data being that associated with the cache miss;  
(b) in response to the request, using the memory interface to fetch the first data from the memory, and  
sending the first data to the processor;  
(c) sending, from the memory interface and via the first bus, the first data and additional data, the  
15 additional data being that stored in the memory adjacent the first data;  
(d) updating the cache with the first data and the additional data via the first bus; and  
(e) updating flags in the cache associated with the first data and the additional data, such that the updated  
first data and additional data in the cache is valid.
- 20 2. A method according to claim 1, wherein the processor is configured to attempt a cache update with the  
first data upon receiving it from the memory interface, the method further including the step of preventing the  
attempted cache update by the processor from being successful, thereby preventing interference with the cache  
update of steps (d) and/or (e).
- 25 3. A method according to claim 2, wherein steps (c), (d), and (e) are performed substantially  
simultaneously.
4. A method according to claim 1, wherein steps (d) and (e) are performed by the memory interface.
- 30 5. A method according to claim 1, wherein steps (d) and (e) are performed in response to the processor  
attempting to update the cache following step (c).
6. A method according to claim 5, wherein the memory interface is configured to monitor the processor  
to determine when it attempts to update the cache following step (c).  
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